

FIG.1

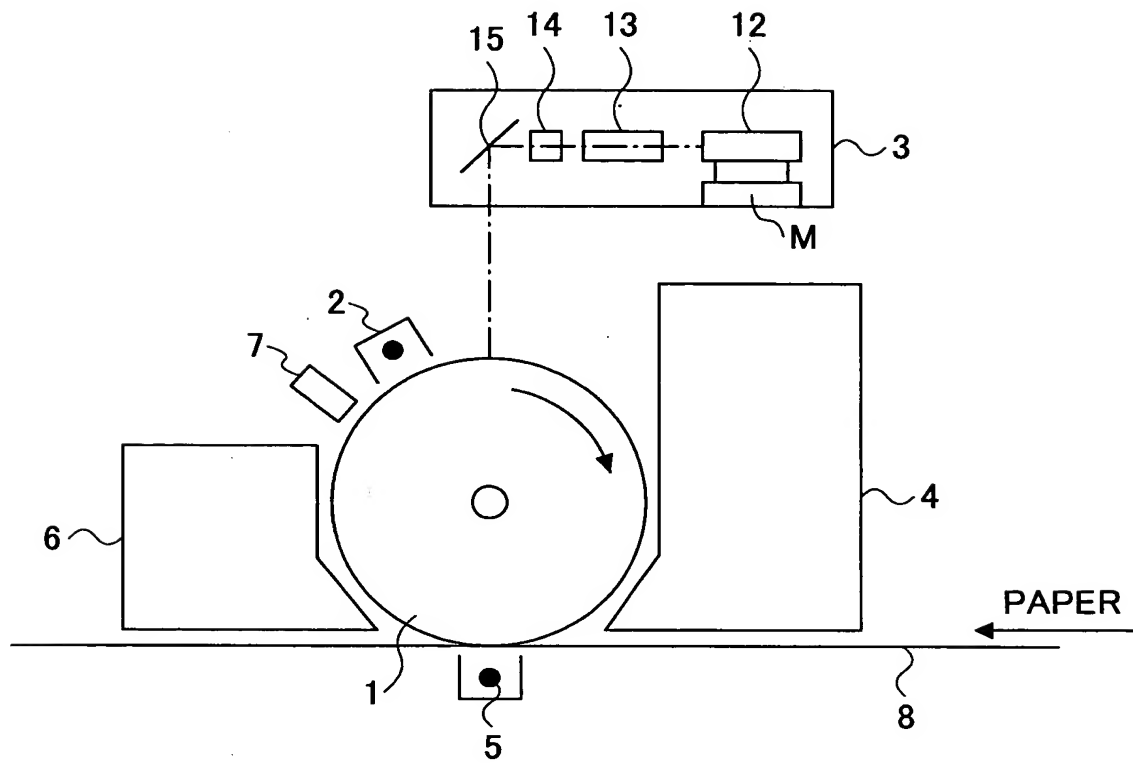


FIG.2

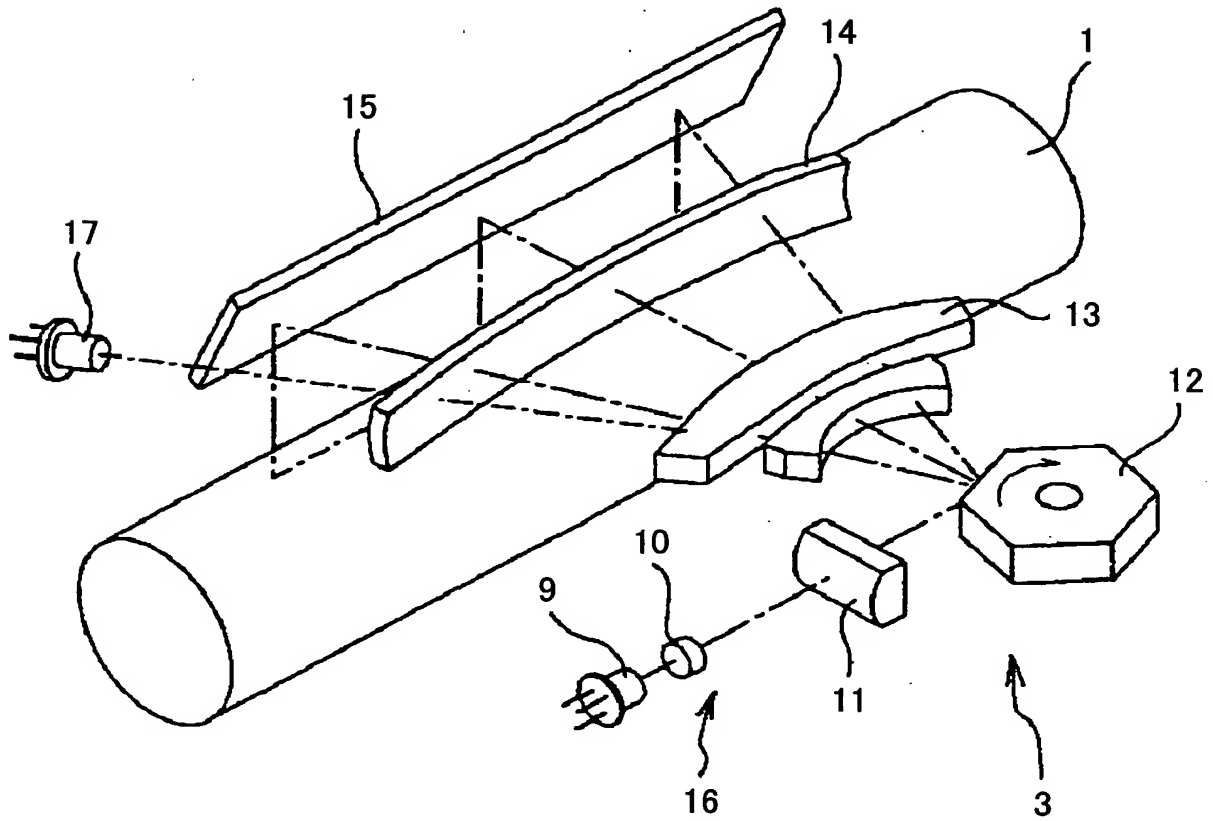


FIG.3

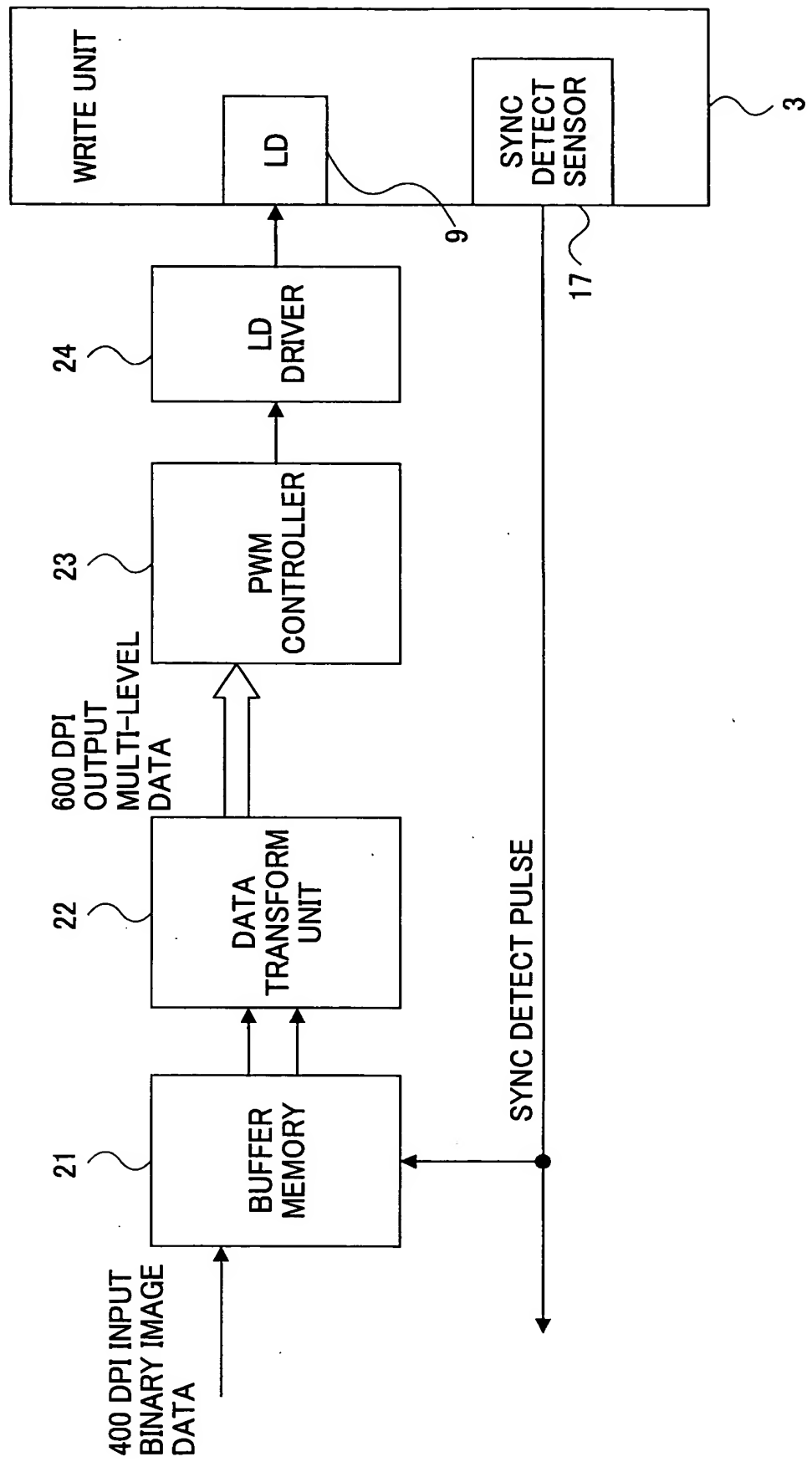


FIG.4

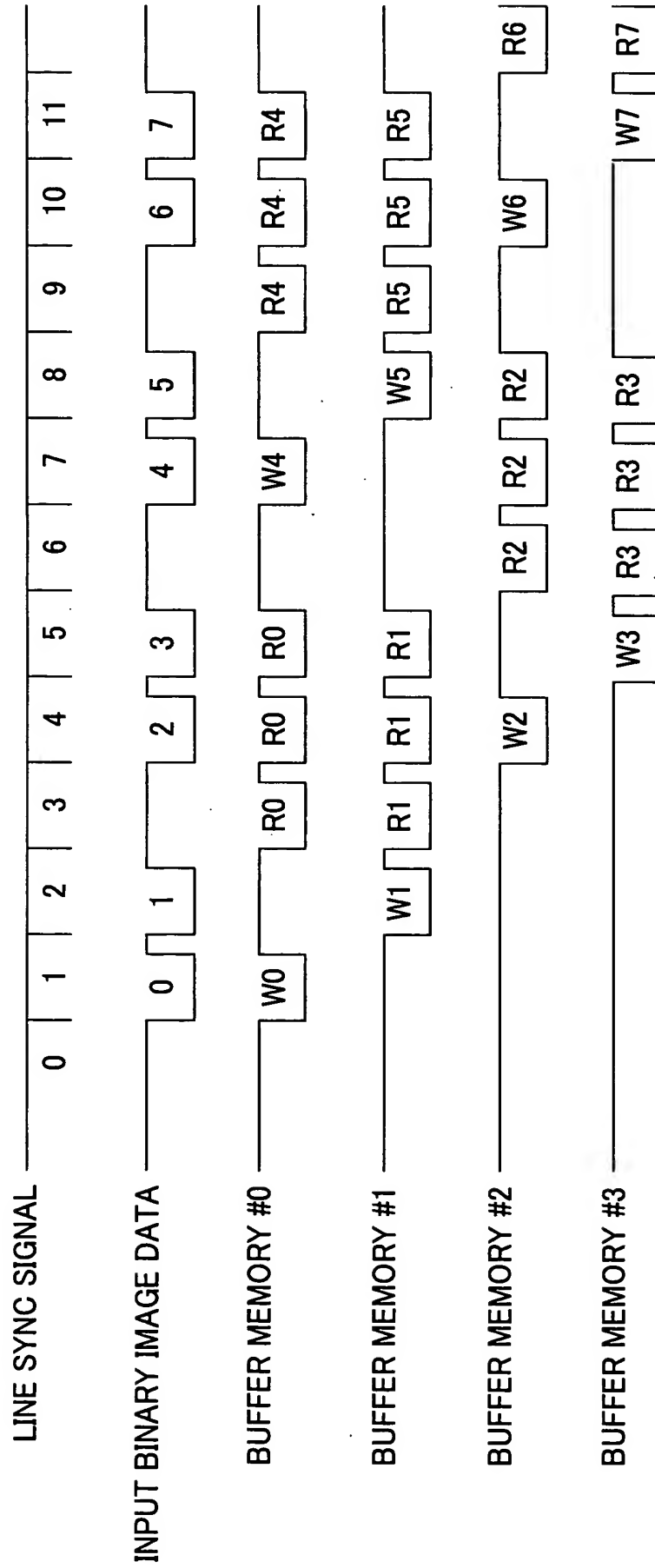


FIG.5

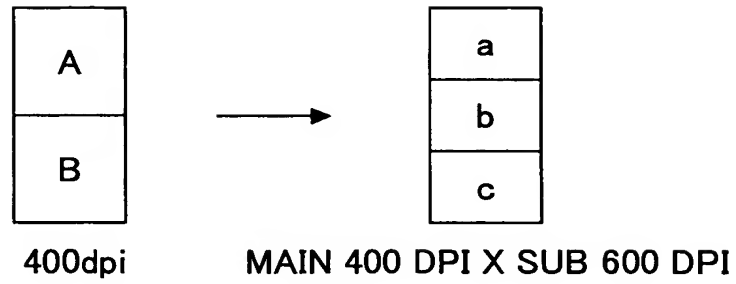


FIG.6

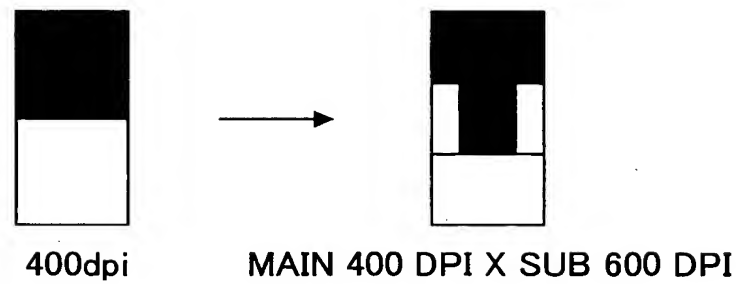


FIG.7

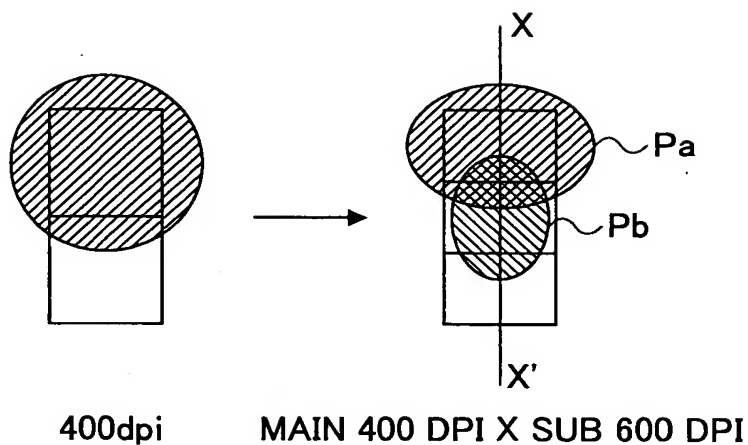


FIG.8

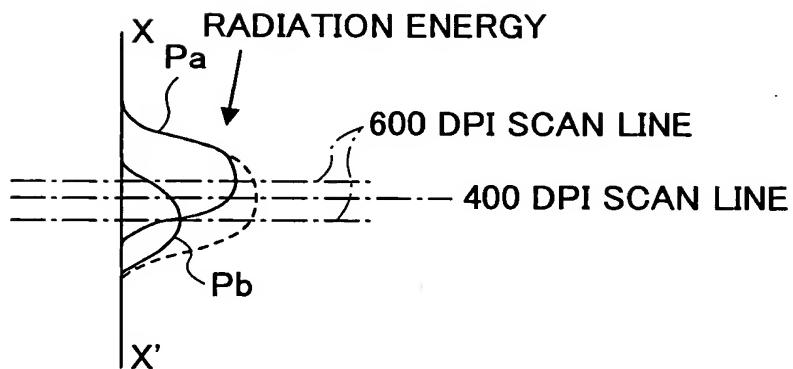


FIG.9

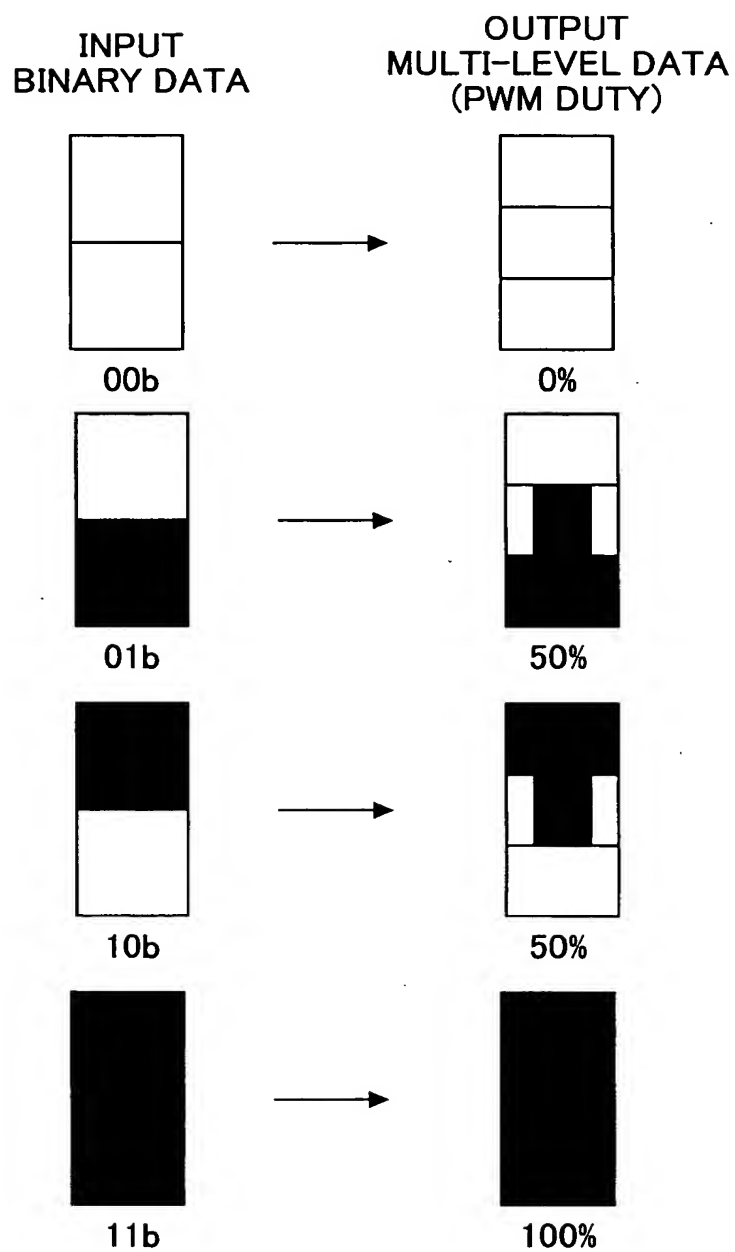


FIG.10A

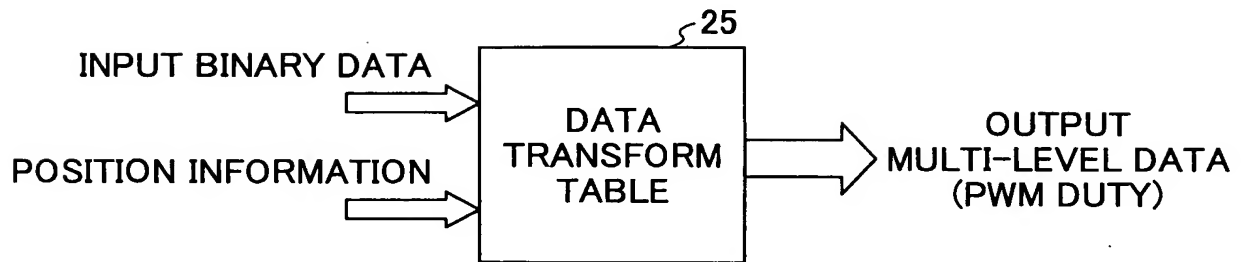


FIG.10B

INPUT BINARY DATA AB	POSITION INFORMATION	OUTPUT MULTI-LEVEL DATA (PWM DUTY)
§	§	§
10	a b c	100% 50% 0%
§	§	§

FIG.11

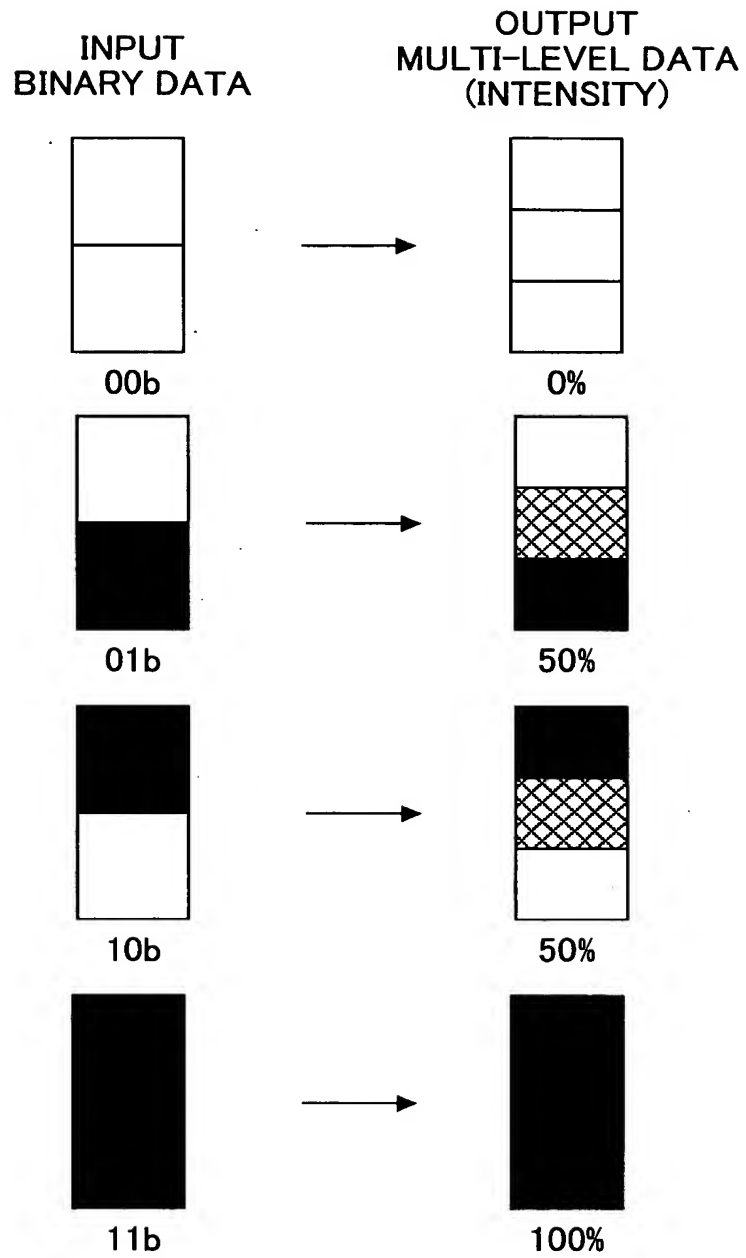


FIG.12

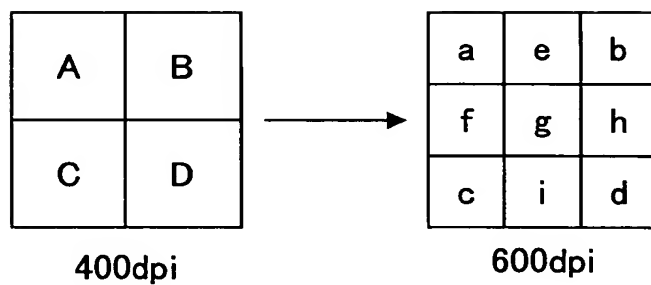


FIG.13

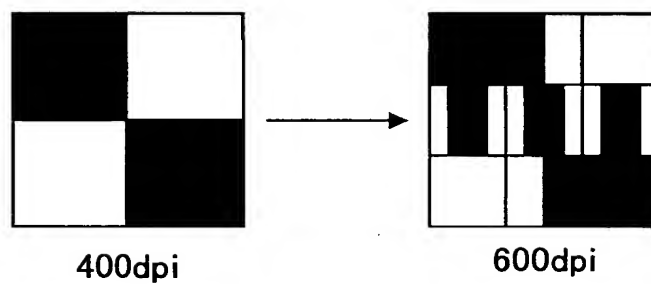


FIG.14

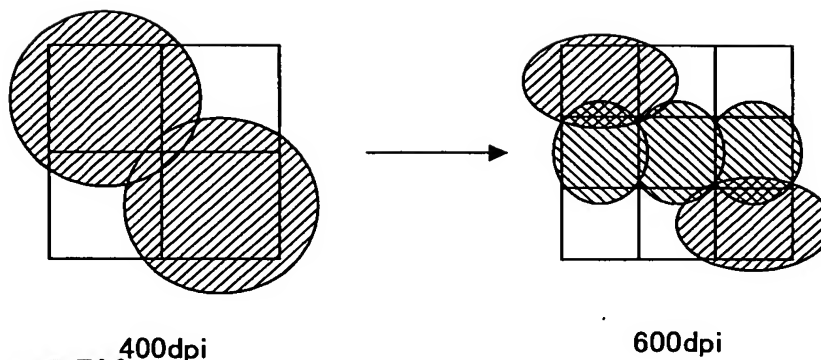
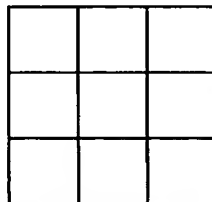
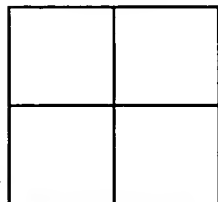


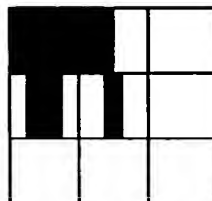
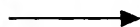
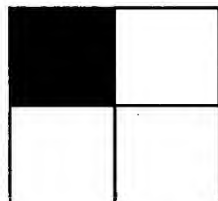
FIG.15

INPUT
BINARY DATA OUTPUT
MULTI-LEVEL DATA

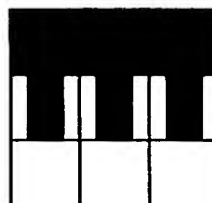
0000b



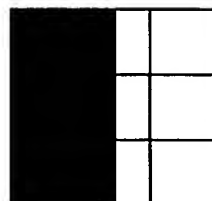
1000b



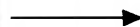
1100b



1010b



1001b



1110b



1111b



BEST AVAILABLE COPY

FIG.16A

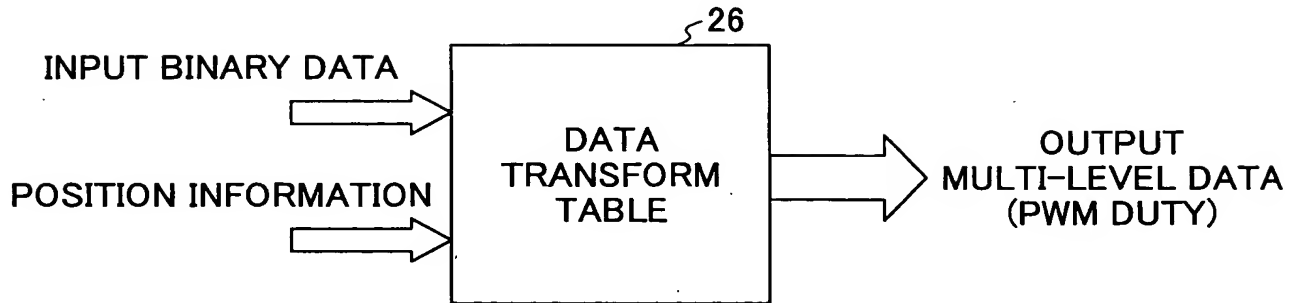


FIG.16B

INPUT BINARY DATA ABCD	POSITION INFORMATION	OUTPUT MULTI-LEVEL DATA (PWM DUTY)	PHASE
Σ	Σ	Σ	Σ
1110	a b c d e f g h i	100% 100% 100% 0% 100% 100% 75% 50% 50%	— — — — 0 — -1 — -1
Σ	Σ	Σ	Σ

FIG.17

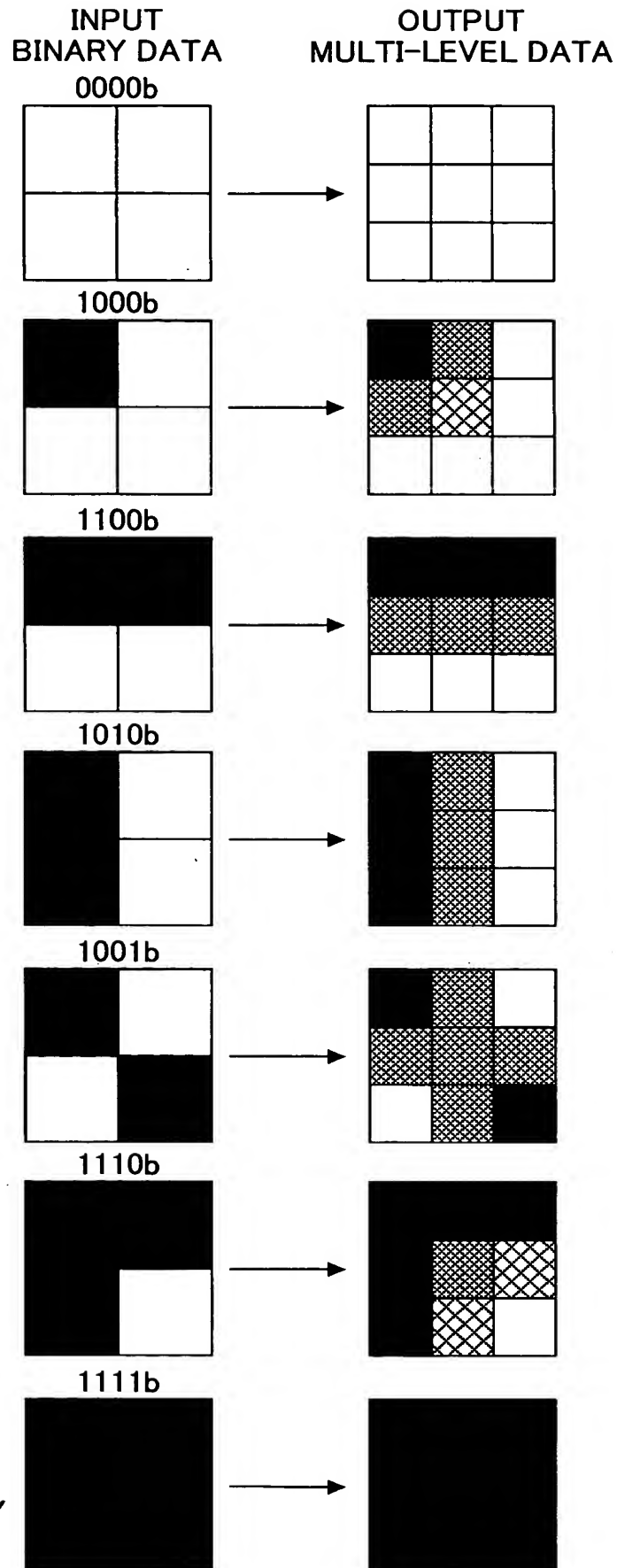


FIG.18

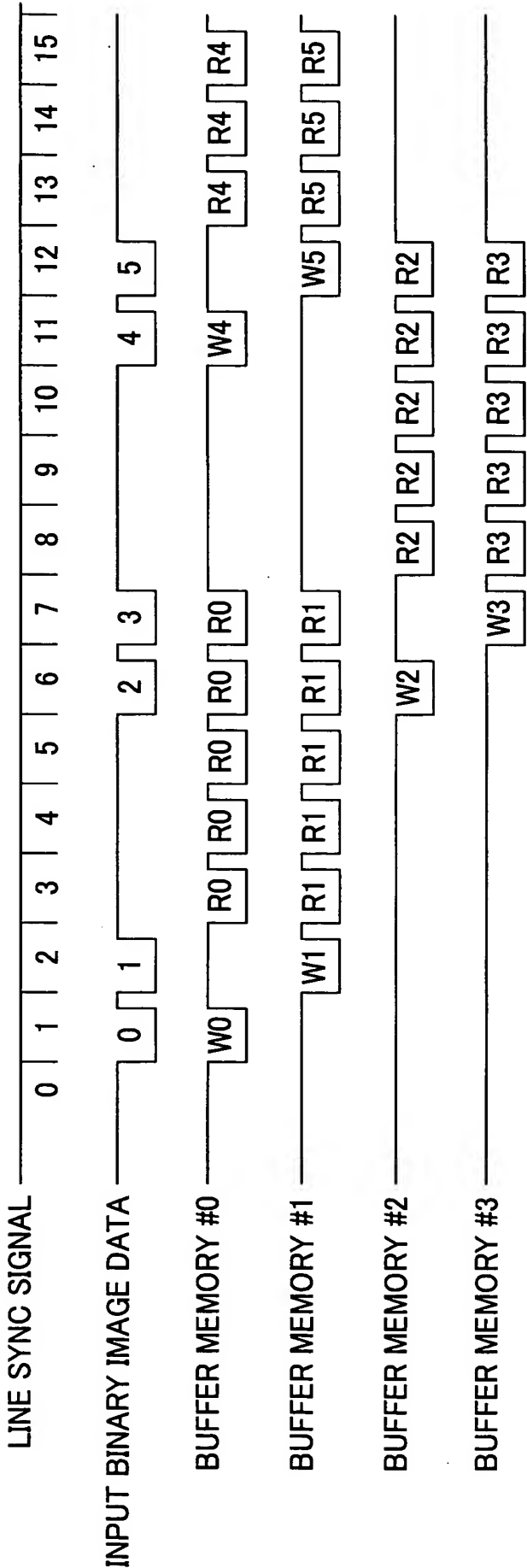


FIG.19

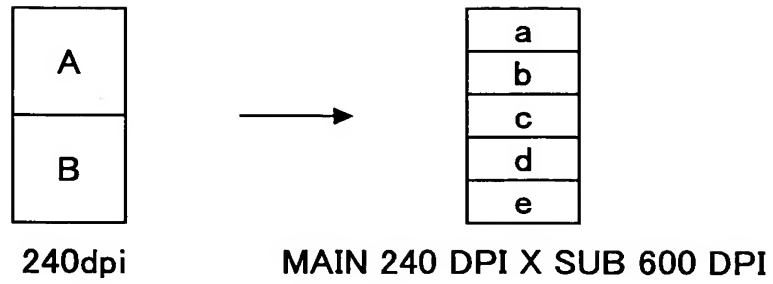


FIG.20

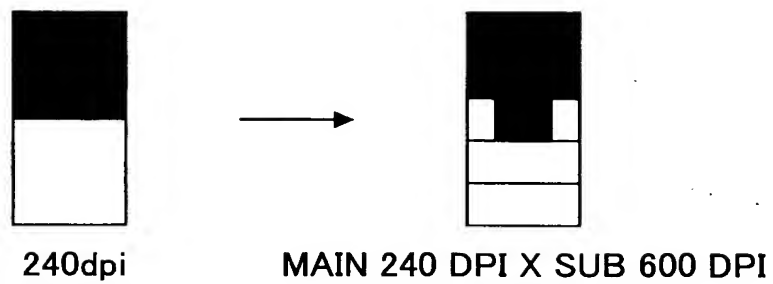


FIG.21

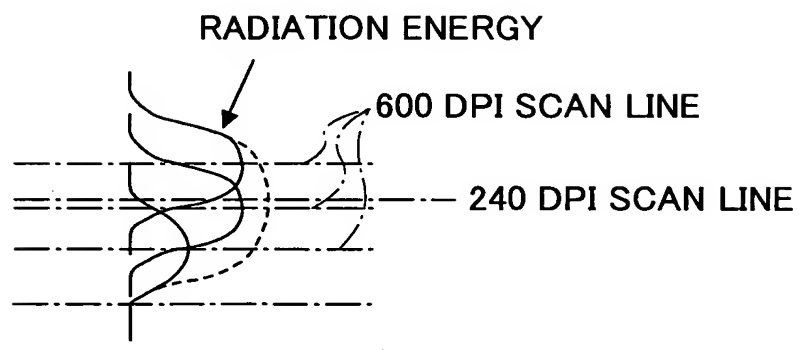


FIG.22

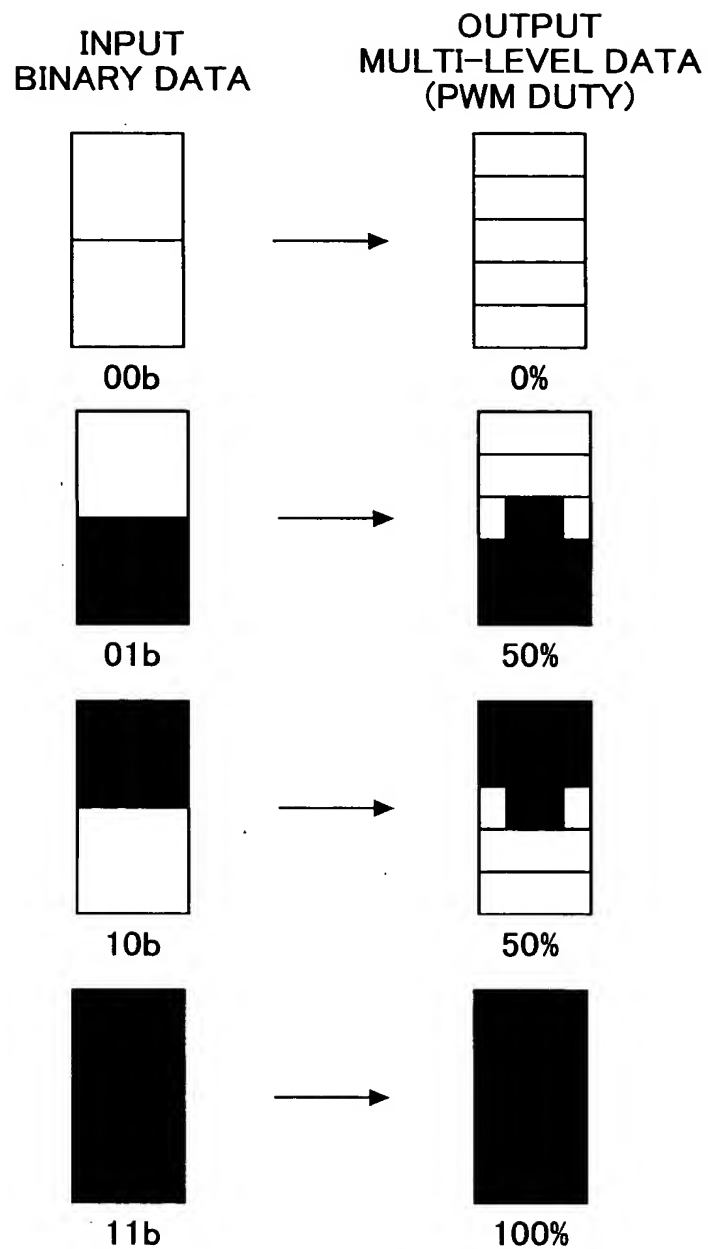


FIG.23

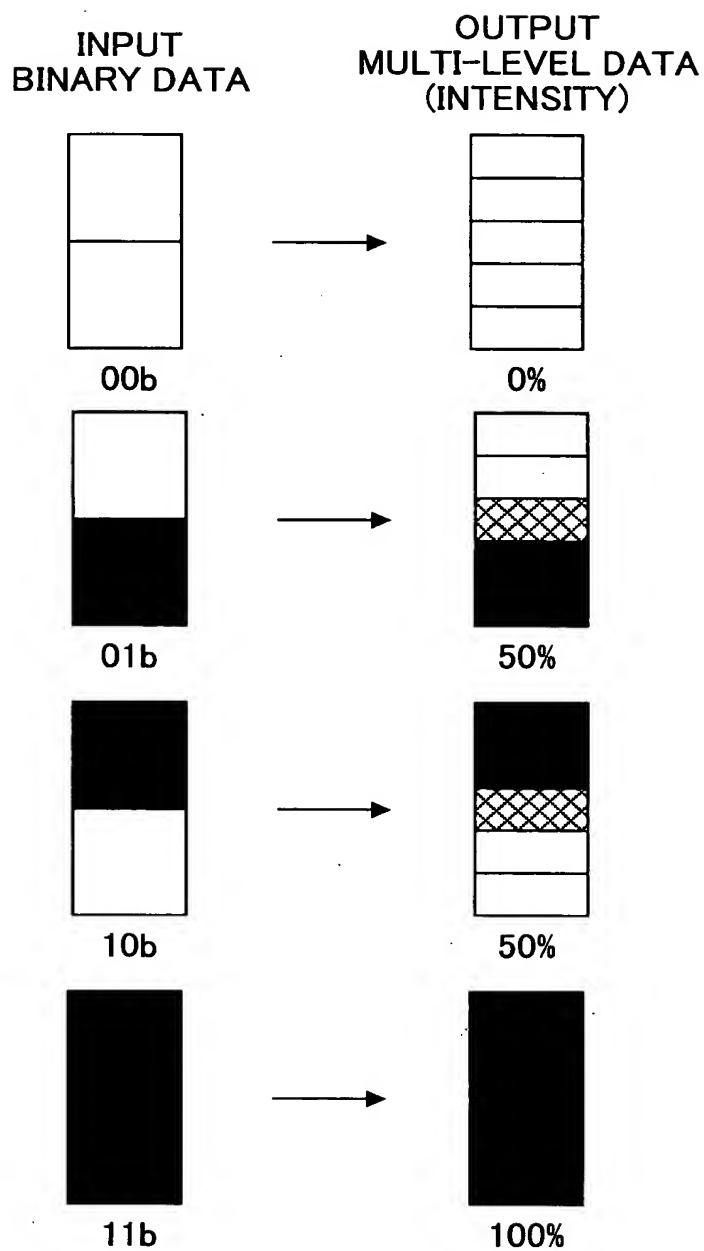


FIG.24

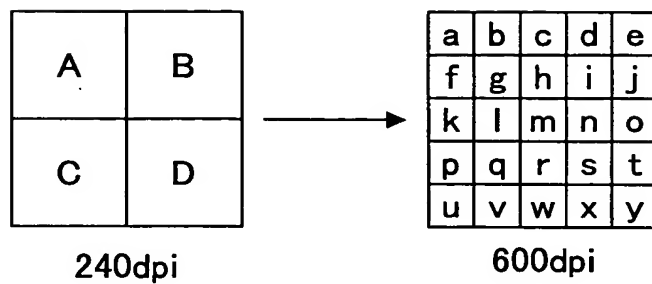


FIG.25

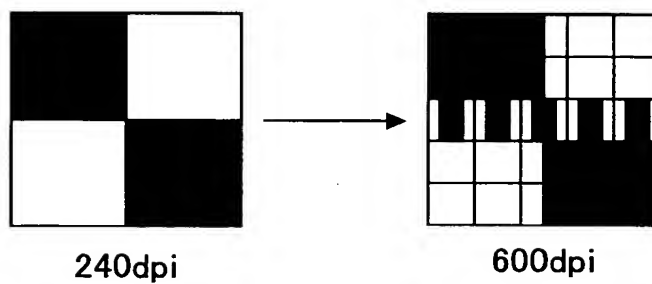
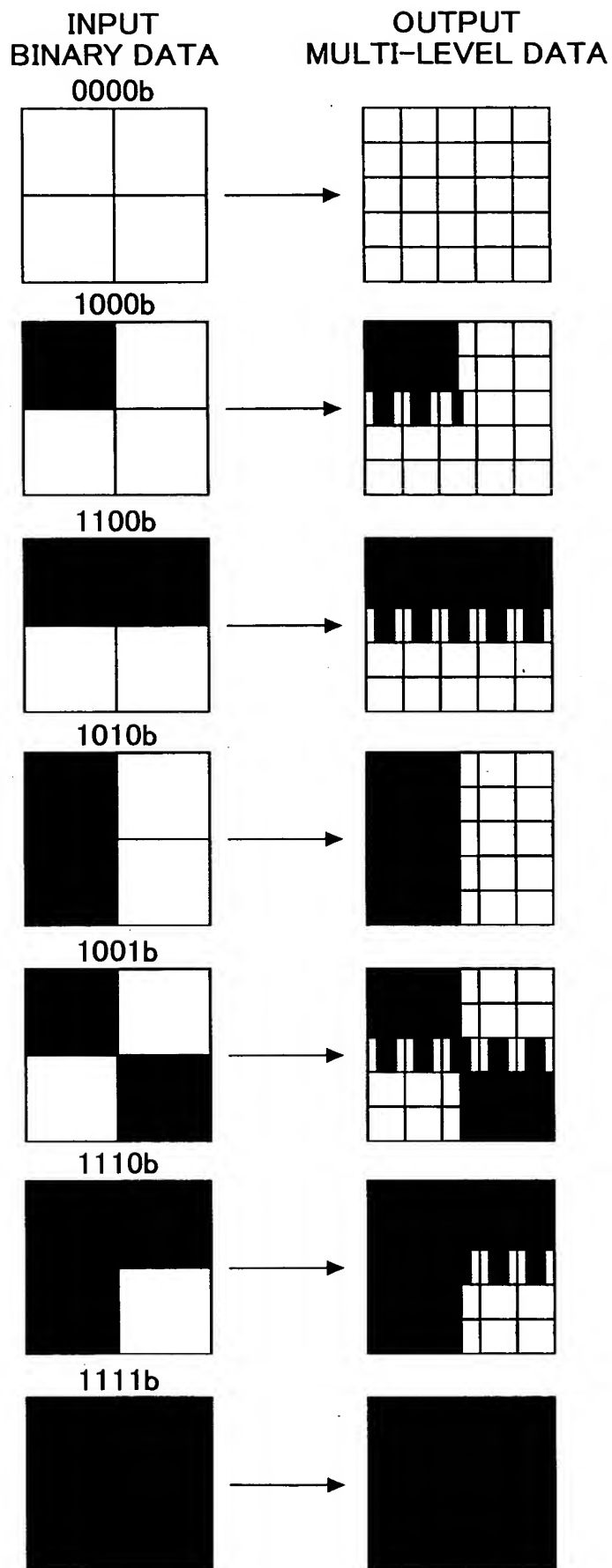


FIG.26



BEST AVAILABLE COPY

FIG.27

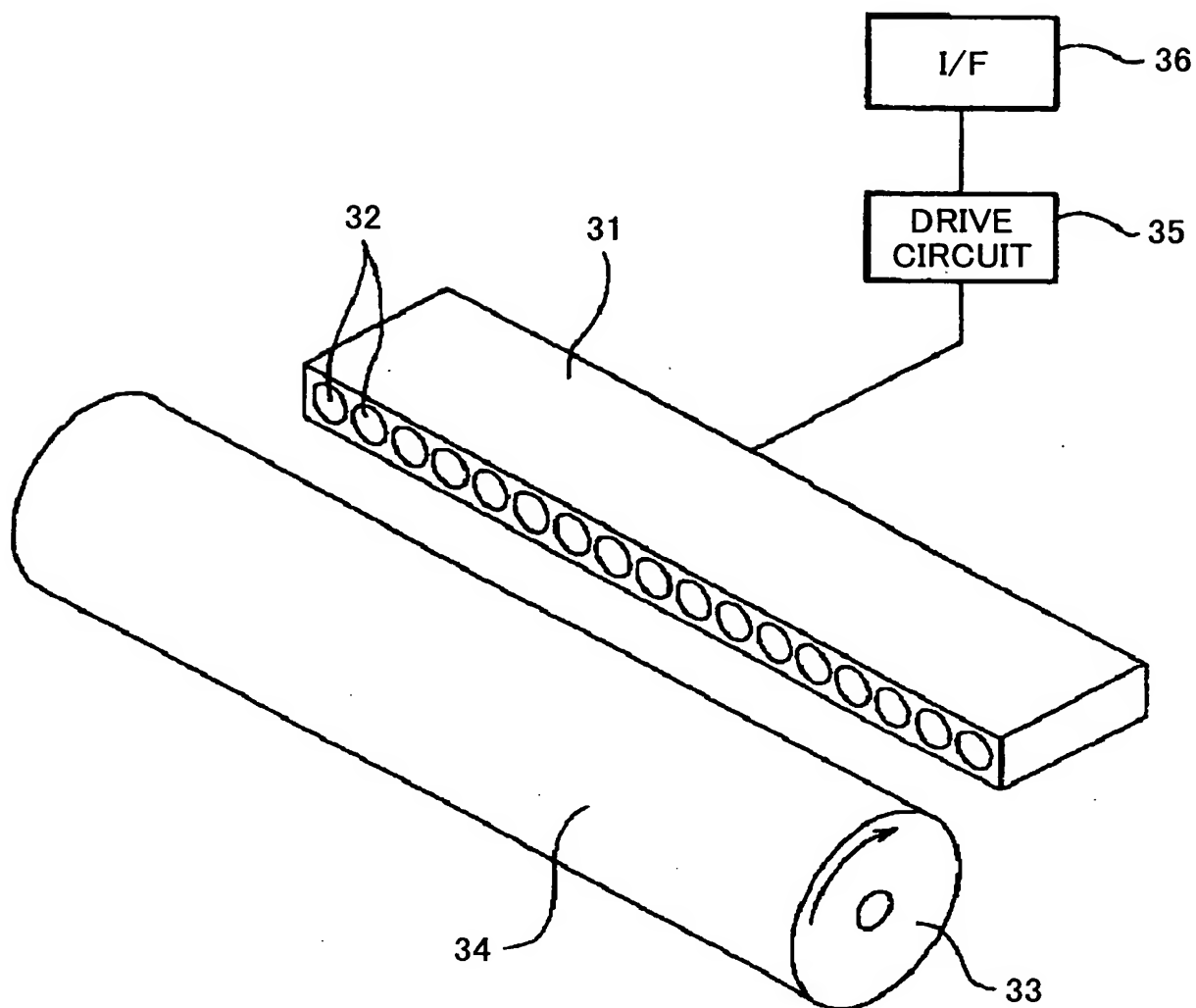


FIG.28

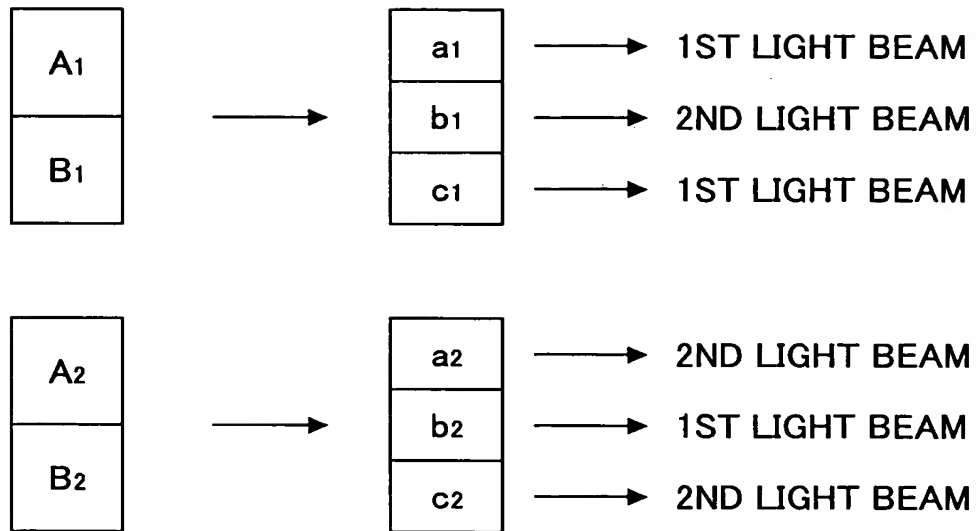


FIG.29

